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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/646,538	08/22/2003	Yan Chong	015114-067000US	9720

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EXAMINER	
LE, THONG QUOC	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/646,538	CHONG ET AL.	
	Examiner	Art Unit	
	Thong Q. Le	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-10* is/are allowed.

6)☒ Claim(s) *11-16 and 19* is/are rejected.

7)☒ Claim(s) *17 and 18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-19 are presented for examination.

Information Disclosure Statement

2. This office acknowledges receipt of the following items from the Applicant:

Information Disclosure Statement (IDS) filed on April 08,2004.

3. Information disclosed and list on PTO 1449 was considered.

Specification

4. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

6. Claims 11-15, 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Asson et al. (U.S. Patent No. 6,492,833).

Regarding claim 11, Asson et al. disclose. a programmable integrated circuit (Figure 2) configured to implement a user design and operated according to the user design in a user mode (Column 1, lines 38-50), the programmable integrated circuit comprising:

a first memory block (Figure 2, 220, Figure 4, 422a);

a control block (Figure 4, 430) that provides a first enable signal prior to the user mode;

a first register (Figure 4, 216a) that stores first data bits prior to the user mode if the first enable signal is in a first state ; and

a first multiplexer (218a) that couples to an output of the first register to a data input of the first memory block if the first enable signal is in the first state, wherein the first data bits are preloaded into the first memory block prior to the user mode only if the first multiplexer selects the first data bits (column 6, lines 25-67).

Regarding claims 12-16, 19, Asson et al. disclose a second memory block (Figure 1, 140), wherein the control block provides a second enable signal prior to the user mode (ABSTRACT); a second register that stores second data bits prior to the user mode if the second enable signal is in a first state (Column 2, lines 1-10); and a

second multiplexer (Figure 2, 218) that couples an output of the first register to a data input of the second memory block if the second enable signal is in the first state, and the second data bits are preloaded into the second memory block prior to the user mode only if the second multiplexer selects the second data bits, and wherein the first multiplexer selects second data bits transmitted from logic elements (Figure 1, LE) when the first enable signal is in a second state during the user mode, and a plurality shift registers (Figure 2, 216) that convert the first data bits to parallel data, outputs of the shift registers being coupled to inputs of the first register (Figures 4-5), and a second multiplexer coupled to programmably select a first clock signal or a second clock signal in response to the first enable signal to provide a selected clock signal, wherein the selected clock signal controls shifting of the first data bits through the shift registers, and further comprising a second multiplexer coupled to programmably select a first clock signal or a second clock signal in response to the first enable signal to provide a selected clock signal, wherein the selected clock signal controls loading data bits into the first memory block, and a second multiplexer coupled to a read/write input of the first memory block that programmably selects a supply voltage (Figure 4, 408, Figure 2,220) or a read/write signal in response to the first enable signal, wherein the second multiplexer selects the supply voltage prior to the user mode when the enable signal is in the first state.

Allowable Subject Matter

7. Claims 1-10 are allowed.

The following is an examiner's statement of reasons for allowance:

Claims 1-10 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Asson et al. (U.S. Patent No. 6,492,833), and others, does not teach the claimed invention having a method for storing data into memory blocks on a programmable integrated circuit configured to implement a user design and operated according to the user design in a user mode as claims 1-10 disclose.

8. Claims 17-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claims 17-18 include allowable subject matter since the prior art made of record and considered pertinent to the applicant's disclosure does not teach or suggest the claimed limitations. Asson et al. (U.S. Patent No. 6,492,833), and others, does not teach the claimed invention having wherein the second multiplexer programmably selects the first memory addresses or second memory addresses transmitted from one or more logic elements in response to the first enable signal.

Conclusion

9. Figures 8, 12-13 in Veenstra et al. (U.S. Patent No. 6,286,114) are very similarly with present invention.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thong Q. Le whose telephone number is 571-272-1783. The examiner can normally be reached on 8:00am-5:00pm M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David C. Nelms can be reached on 571-272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thong Q. Le
Primary Examiner
Art Unit 2818

THONG LE
PRIMARY EXAMINER